Atty. Docket No.: LAYADI 28-36 PATENT APPLICATION

METHOD FOR REDUCING A METAL SEAM IN AN INTERCONNECT STRUCTURE AND A DEVICE MANUFACTURED THEREBY

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to forming an interconnect structure and, more specifically, to a method for reducing a metal seam in an interconnect structure and a device manufactured by that method.

BACKGROUND OF THE INVENTION

[0002] Devices in the semiconductor industry continue to advance toward higher performance, while maintaining or even lowering the cost of manufacturing. Micro-miniaturization of semiconductor devices has resulted in higher performance, through increases in transistor speed and in the number of devices incorporated in a chip; however, this trend has also increased yield and reliability failures. As contact or via openings decrease in size, the aspect ratio, or the ratio of the depth of the opening to the diameter of the opening, also increases. With a higher aspect ratio, the use of aluminum-based metallization to fill the contact opening, results in electromigration and reliability failures. To alleviate

reliability failures, the semiconductor industry has evolved to the use of tungsten, in certain device, for filling narrow, deep contact or via openings.

[0003] The switch to tungsten filled contact openings takes advantage of the improved conformal, or step, coverage that results from the use of a plasma enhanced chemical vapor deposition (PECVD) process. In addition, tungsten's high current carrying characteristics reduce the risk of electromigration failure. The conventional method of forming tungsten plugs in vias includes plasma etching of vias or contacts, photoresist striping and cleaning, adhesion layer and barrier metal deposition by physical vapor deposition (PVD) and tungsten deposition by PECVD. Typical adhesion and barrier materials used may consist of a stack of titanium and titanium nitride, respectively. The titanium reduces the contact resistance of the interconnect, and the titanium nitride is a protective layer against titanium attack by a tungsten hexaflouride gas that is used during tungsten deposition. In addition, tungsten adheres to titanium nitride very well, resulting in a mechanically stable tungsten plug. After tungsten plug filling, voids, or so-called tungsten seams, are often observed in the tungsten material. This is particularly the case, when the etched via profiles are straight. Such tungsten seams are commonly exposed during subsequent processing, such as during processes

designed to remove unwanted tungsten from regions other then the contact opening. Moreover, in certain situations the size of the tungsten seam is increased due to exposure to the removal process. This often creates a difficult topology for subsequent metallization coverage as well as electrical device degradation, which is especially apparent as leakage in metal-oxide-metal MOM capacitor structures. Therefore, processes have been developed, either attempting to create seamless tungsten contact opening fills or repairing the seam or void in the tungsten fill. For example, one attempt involves altering the via etch profile so as to assume a tapered profile, thereby reducing the tungsten seam and allowing better tungsten fill. The tapered via profile helps reduce many of the tungsten seam issues, however, it often leads to increased contact resistance, which is also very undesirable.

[0004] Accordingly, what is needed in the art is an interconnect structure and method of manufacture therefor that does not experience the tungsten "seam" problems, as experienced in the prior art.

SUMMARY OF THE INVENTION

[0005] To address the above-discussed deficiencies of the prior art, the present invention provides a method of manufacturing an interconnect structure. In an advantageous embodiment, the method includes forming a nucleation layer, including a first metal, over a barrier layer and within an opening formed in a dielectric layer. The method further includes forming an intermediate layer, including a second metal such as titanium nitride, over the nucleation layer and within the opening, and forming a plug portion layer, including the first metal, over the intermediate layer and within the opening. In one advantageous embodiment, the nucleation layer is tungsten and the intermediate layer is titanium nitride.

[0006] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do

not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The invention is best understood from the following detailed description when read with the accompanying FIGUREs. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0008] Prior Art FIGURE 1 illustrates a partial sectional view of a conventional interconnect structure, including an undesirable tungsten seam within a tungsten plug;

[0009] FIGURE 2 illustrates one embodiment of a partially completed integrated circuit, including an interconnect structure in accordance with the present invention;

[0010] FIGURE 3 illustrates a cross-sectional view of a partially completed interconnect structure according to the present invention;

[0011] FIGURE 4 illustrates the partially completed interconnect structure illustrated in FIGURE 3, after formation of a nucleation layer comprising a first metal;

[0012] FIGURE 5 illustrates the partially completed interconnect

structure illustrated in FIGURE 4, after formation of an intermediate layer over the nucleation layer;

[0013] FIGURE 6 illustrates the partially completed interconnect structure illustrated in FIGURE 5, after formation of a plug portion layer over the intermediate layer;

[0014] FIGURE 7 illustrates an example of a partially completed interconnect structure, containing a plurality of nucleation layers and a plurality of intermediate layers; and

[0015] FIGURE 8 illustrates a partial sectional view of an integrated circuit into which the completed interconnect structure (FIGURE 2) may be incorporated.

DETAILED DESCRIPTION

[0016] Referring initially to Prior Art FIGURE 1, illustrated is a partial sectional view of a conventional integrated circuit 100 at an intermediate stage of manufacture. The conventional integrated circuit 100 includes a substrate 110, an n-channel metal oxide semiconductor (NMOS) or a p-channel metal oxide semiconductor (PMOS) tub 120, source and drain regions 130, field oxide regions 140, a gate oxide 150, a gate electrode 160, and a dielectric layer 170.

[0017] Also illustrated in Prior Art FIGURE 1 is a conventional tungsten plug 185 located within a contact opening 180 within the dielectric layer 170. The tungsten plug 185 was formed using traditional formation processes, and as illustrated, includes a conventional titanium/titanium nitride barrier layer 186 located thereunder. Oftentimes, to inhibit an attack of the titanium within the titanium/titanium nitride barrier layer 186 by the tungsten hexafluoride used to form the tungsten plug 185, silane is mixed with tungsten hexafluoride. Unfortunately, however, the silane causes grains within the tungsten plug 185 to become undesirably large. The undesirably large grains tend to inadequately fill the high aspect ratio contact opening 180, which results in an unwanted tungsten seam 190.

[0018] Additionally, subsequent processing steps may ultimately expose the tungsten seam 190, creating a tungsten seam opening 195. The tungsten seam opening 195 is particularly disadvantageous, because trapped particles, such as trapped residual slurry particles resulting from a chemical mechanical polishing (CMP) process, may provide yield and contact resistance issues. In the case when a metal oxide metal (MOM) capacitor is deposited on top of the tungsten plug 185, the undesirable tungsten seam opening 195 may induce capacitor leakage and MOM reliability failure.

[0019] Turning now to FIGURE 2, illustrated is one embodiment of a partially completed integrated circuit 200, including an interconnect structure 260 in accordance with the present invention. As illustrated in FIGURE 2, the partially completed integrated circuit 200 includes a wafer substrate 210 having a tub region 215 located therein. The tub region 215 may comprise a tub for a convention n-channel metal oxide semiconductor (NMOS) device, or in an alternative embodiment, a tub for a conventional p-channel metal oxide semiconductor (PMOS) device. Further located within the wafer substrate 210 are conventional source/drain regions 220 and field oxide regions 225. Located over the wafer substrate 210, in the embodiment illustrated in FIGURE 2, is a gate structure 230, including a gate oxide 235 and a gate electrode 240.

[0020] Located within a dielectric layer 250 formed over the

gate structure 230, is the previously mentioned interconnect structure 260. As illustrated, the interconnect structure 260 includes a barrier layer 265 formed within a contact opening 255 in the dielectric layer 250. In one advantageous embodiment, the contact opening 255 may be a via formed in a dielectric layer between two metal layers.

[0021] The interconnect structure 260 further includes a nucleation layer 270, comprising a first metal such as tungsten, located over the barrier layer 265. Located over the nucleation layer 270 is an intermediate layer 275, which comprises a second metal, for example titanium nitride. As is illustrated, the intermediate layer 275 is also located within the contact opening 255. The interconnect structure 260 further includes a plug portion layer 280, comprising the first metal, and located over the intermediate layer 275.

[0022] The interconnect structure 260 benefits from breaking the formation thereof into at least two phases. Because thinner layers are being formed, mainly the nucleation layer 270 and the plug portion layer 280, a reduced grain growth may be achieved. Additionally, by restricting the grain growth of the layers in this way, a fine grain material with a reduced "seam," may be advantageously manufactured.

[0023] Turning to FIGUREs 3-7, with continued reference to

FIGURE 2, illustrated are detailed manufacturing steps illustrating how one might manufacture the interconnect structure 260 depicted in FIGURE 2. FIGURE 3 illustrates a cross-sectional view of a partially completed interconnect structure 300 according to the present invention. The partially completed interconnect structure 300 illustrated in FIGURE 3 includes a dielectric layer 310, such as an interlevel dielectric layer located over a gate structure, having a contact opening 315 formed therein. One skilled in the art understands how to form such a contact opening 315, including using conventional photolithographic and etching techniques.

[0024] Optionally formed within the contact opening 315 is an adhesion layer 320. The adhesion layer 320 is advantageously designed to provide any necessary adhesion between the dielectric layer 310 and any subsequently formed layer. The adhesion layer 320 may be formed using varying manufacturing techniques and parameters, however, in one particularly advantageous embodiment, the adhesion layer 320 is formed using a conventional chemical vapor deposition (CVD) process. Likewise, the adhesion layer 320 may comprise various materials and thicknesses. For example, in one particular embodiment the adhesion layer 320 comprises titanium (Ti) or tantalum (Ta), and has a thickness ranging from about 5 nm to about 20 nm. While the adhesion layer 320 is shown in FIGURE 3, one skilled in the art understands that it is only optional, and

should not limit the present invention in any way.

[0025] Advantageously located over the optional adhesion layer 320 is a barrier layer 325. The barrier layer 325 in the illustrative embodiment shown in FIGURE 3 comprises titanium nitride and has a thickness ranging from about 5 nm to about 50 nm. It should be noted, however, that the barrier layer 325 may comprise other materials, including tantalum nitride, tungsten nitride or another suitable material. Similar to the adhesion layer 320, the barrier layer 325 may be formed using conventional deposition processes well known to those who are skilled in the art, such as CVD or physical vapor deposition (PVD) processes.

[0026] Turning now to FIGURE 4, illustrated is the partially completed interconnect structure 300 illustrated in FIGURE 3, after formation of a nucleation layer 410 comprising a first metal. As illustrated, the nucleation layer 410 is formed over the barrier layer 325 and may have a thickness ranging from about 20 nm to about 200 nm, depending on a width of the contact opening 315. In one particular advantageous embodiment, the nucleation layer 410 should be about half a total amount of the first metal thickness in the completed interconnect structure 260 (FIGURE 2).

[0027] In the illustrative embodiment shown in FIGURE 4, the first metal is tungsten, however, one skilled in the art understands that other similar materials that are currently known

or hereafter discovered, may comprise the first metal, an therefore the nucleation layer 410. In the particular embodiment where the first metal comprises tungsten, the nucleation layer 410 may be formed with a gas mixture of tungsten hexafluoride and silane. A plasma enhanced chemical vapor deposition (PECVD) process, using temperatures ranging from about 400°C to about 500°C, may be used to deposit the nucleation layer 410, in which case the tungsten hexafluoride is used as a source. The process of tungsten deposition starts by the formation of small nuclei or "islands" on the barrier layer 325. In an ideal case, the surface of the barrier layer 325 will eventually be covered by the same size of small and uniform individual nuclei. As the nucleation continues, the individual nuclei touch each other, and coalesce as they continue to grow, finally beginning to form a continuous film. At this point, the deposition is discontinued, providing the illustrated nucleation layer 410.

[0028] Turning now to FIGURE 5, illustrated is the partially completed interconnect structure 300 illustrated in FIGURE 4, after formation of an intermediate layer 510 over the nucleation layer 410. The intermediate layer 510, which comprises a second metal, is desirably formed to a thickness of less than about 20 nm, and even more desirably, formed to a thickness ranging from about 5 nm to about 20 nm. Although advantageous embodiments of the present

invention provide for an intermediate layer 510 with a thickness of less than about 20 nm, the thickness of the intermediate layer 510 may depend on the size of the contact opening 315 and is, thus, not necessarily limited to this range.

[0029] One embodiment of the present invention includes the second metal comprising a nitride, such as titanium nitride. While titanium nitride may be a preferred embodiment, other similar second metals, such as tantalum nitride and tungsten nitride, are also within the scope of the present invention. The intermediate layer 510 may be formed using similar manufacturing techniques as for the nucleation layer 410, such as a conventional CVD process or other similar process. The deposition of the intermediate layer 510 provides a relatively smooth surface on which a subsequent layer may be formed. The smooth surface inhibits the formation of the larger grain sizes, and thus, allows the plug to form without the seam often generated by prior art processes.

[0030] Turning to FIGURE 6, illustrated is the partially completed interconnect structure 300 illustrated in FIGURE 5, after formation of a plug portion layer 610 over the intermediate layer 510. The plug portion layer 610 comprises a similar material as the nucleation layer 410. Thus, in various embodiments, the plug portion layer 610 may comprise tungsten or another similar material.

[0031] In the embodiment illustrated above, where the nucleation layer 410 has a thickness that is half the overall thickness of the first metal within the completed interconnect structure 260 (FIGURE 2), the plug portion layer 610 would provide the other half of the overall thickness of the first metal within the completed interconnect structure 260. Thus, in the embodiment illustrated above, if the overall thickness of the first metal within the completed interconnect structure 260 is 40 nm, the nucleation layer would have a thickness of about 20 nm and the plug portion layer would have a thickness of about 20 nm. The ratio should hold the same, if the width of the contact opening 315 were increased, and the same number of layers (e.g., nucleation layer 410 and plug portion layer 610) comprise the first metal. In a particularly advantageous embodiment, the nucleation layer 410 and the plug portion layer 610 are formed such that an average grain size of the nucleation layer 410 is substantially the same size as an average grain size of the plug portion layer 610.

[0032] The plug portion layer 610 may be formed using similar manufacturing techniques as intermediate layer 510, nucleation layer 410, adhesion layer 320 and barrier layer 325. In one embodiment, the partially completed interconnect structure 300 is maintained in a single multi-chamber tool, only varying the gas composition in the various chambers to form the adhesion layer 320,

barrier layer 325, nucleation layer 410, intermediate layer 510 and plug portion layer 610, respectively. Subsequent to forming the plug portion layer 610, a conventional chemical mechanical planarization (CMP) process, or another similar process, may be used to planarize the partially completed interconnect structure 300 illustrated in FIGURE 6, resulting with the completed interconnect structure 260 illustrated in FIGURE 2.

[0033] While the present invention has been disclosed above as only having one nucleation layer 410 and one intermediate layer 510, the present invention is not restricted to having only one of each layers. In some cases, it may be advantageous to use more than one nucleation layer 410 and intermediate layer 510, to further reduce the tungsten grain size.

[0034] Turning to FIGURE 7, illustrated is an example of a partially completed interconnect structure 700, containing a plurality of nucleation layers 710a, 710b and a plurality of intermediate layers 720a, 720b. The thicknesses of the nucleation layer 710a, 710b and intermediate layers 720a, 720b, would vary according to the number of layers. For example, if the overall thickness of the first metal within the completed interconnect structure 260 (FIGURE 2) were 45 nm, and only two nucleation layers (e.g., first nucleation layer 710a and second nucleation layer 710b) were used, the first nucleation layer 710a would desirably

have a thickness of about 15 nm, the second nucleation layer 710b would desirably have a thickness of about 15 nm and a plug portion layer 730 would desirably have a thickness of about 15 nm. While only two nucleation layer 710a, 710b and intermediate layers 720a, 720b are illustrated in FIGURE 7, it should be understood that numerous nucleation layers and intermediate layers are within the scope of the present invention.

[0035] Turning now to FIGURE 8, there is illustrated a partial sectional view of an integrated circuit 800 into which the completed interconnect structure 260 (FIGURE 2) may be incorporated. The integrated circuit 800 may include active devices, such as transistors, used to form CMOS devices, BiCMOS devices, Bipolar devices, or other types of active devices. The integrated circuit 800 may further include passive devices such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of device and their manufacture.

[0036] In the illustrated embodiment, the integrated circuit 800 includes conventionally formed transistors 810, tubs 820, source/drains 830, gate oxides 840 and gate electrodes 850. The conventional devices 810, such as transistors, can be interconnected by the completed interconnect structures 260. It should be understood that the interconnect 260 may form a contact

plug that contacts the source/drains 830, or the gate electrodes 850. It may also form a via 860 that extends through an interlevel dielectric layer 870 or 875, interconnecting various devices 810 to form an operative integrated circuit.

[0037] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.